REMARKS/ARGUMENTS

1. Request for Continued Examination:

The applicants respectfully request continued examination of the above-indicated application as per 37 CFR 1.114.

2. Rejections over claims 1-20:

Claim 1 was rejected under 35 U.S.C. 103(a), for reasons of record that can be found on pages 3-4 in the Office action identified above, which is Part of Paper No./Mail Date 1205. Claim 1 was rejected by the Examiner under 103 as being unpatentable over Hong et al. (US 6,429,057) in view of Rioux (US 5,554,488).

Hong teaches a method comprising the steps of forming a gate wire including a plurality of gate lines and gate pads by a first photolithography process. The next step is depositing a first insulating layer, a semiconductor layer, an ohmic contact layer and a metal layer on the gate wire and forming a metal layer pattern, an ohmic contact layer pattern, a semiconductor layer pattern and a first insulating layer pattern that have a matrix shape layout overlapping the gate wire except the gate pad by a second photolithography process. The next step is depositing a transparent conductor layer, forming a transparent conductor pattern including a pixel electrode, a plurality of redundant data lines, redundant source electrodes, redundant drain electrodes, redundant data pads and redundant gate pads by a third photolithography process. Following is etching out the portion of the metal layer not covered by the transparent conductor pattern and the ohmic contact layer thereunder, depositing a second insulating layer, forming a passivation layer pattern having openings respectively exposing the gate pad, the data pad, the pixel electrode and the portion of the semiconductor layer connecting the adjacent data line, and etching out the portion of the semiconductor layer exposed through the openings.

Rioux teaches a method of forming a semiconductor structure based on a lift-off masking process. After providing a weakly bonded surface layer on the substrate, a multilayer masking layer stack is deposited, and patterned to define an

opening with undercut sidewalls. The multilayer masking stack forms a heat resistant mask for high temperature deposition of one or more conductive layers, e.g. sputtered metals to form a gate metal stack for a FET. The undercut sidewalls of the mask create a discontinuity in the deposited metal layers. Preferential etching of the deposited metal layers occurs at the discontinuity, resulting in separation of the gate metal structure and the excess metal overlying the masking layers. The weakly bonded surface layer on the substrate controls the adhesion of the overlying masking layers, and allows for the excess metal and the underlying masking layers to be separated from the substrate simply by a liftoff process (See FIGS. 4-10 and col. 6, line 50-col. 8, line 25).

The method disclosed in Rioux reference for forming the tungsten layer 48 with tapered sidewalls is quite different from the claimed invention of this application. None of the cited references, alone or in combination, teaches or makes obvious all of the limitations of "forming a patterned photoresist on said molybdenum-containing metal layer, wherein said patterned photoresist defines a gate and word line array pattern", as required in claim 1. The Examiner has stated no motivation that would cause one reasonably skilled in the art to modify Rioux reference. There is nothing that the applicants can find in the cited reference that would serve as motivation.

Reconsideration of claim 1 is therefore politely requested. As Claims 2-12 are dependent upon claim 1, they should be allowable if claim 1 is allowed. Reconsideration of claims 2-12 is therefore politely requested.

Claim 13 was rejected under 35 U.S.C. 102(e), for reasons of record that can be found on page 2 in the Office action identified above, which is Part of Paper No./Mail Date 1205. Claim 13 was rejected by the Examiner under 102 because of Hong reference. Claim 16 is rejected under 103 as being unpatentable over Hong and Rioux references and in view of Hori reference (US 5,445,710).

Hori teaches a dry-etching method comprising the steps of forming carbon film on a substrate to be etched, forming a resist pattern on the carbon thin film, selectively etching the carbon film using the resist pattern as a mask by a plasma of a gas mixture of a gas containing fluorine atoms and a gas containing oxygen atoms which are mixed at an atomic ratio of fluorine to oxygen of 198:1 to 1:2 so as to form a carbon film pattern, and selectively etching said substrate to be etched using the

carbon film pattern as a mask or the resist pattern and the carbon film pattern as masks. According to Hori's teaching, this method is merely applicable to the etching of carbon film or resist film. The applicants submit that Hori fails to disclose depositing a molybdenum-containing metal layer on a glass substrate.

The applicants believe that the amended claim 13 is allowable because none of the cited references, alone or in combination, teaches or makes obvious all of the limitations of "etching said molybdenum-containing metal layer by using fluorine/oxygen containing gas mixture containing SF_6/O_2 with a ratio of about 700sccm/300sccm, and using said patterned photoresist as an etching mask to form said gate and word line array pattern", as required by the amended claim 13.

As Claims 14-15 and 17-20 are dependent upon claim 1, they should be allowable if claim 13 is allowed. Reconsideration of claims 14-15 and 17-20 is therefore politely requested.

Sincerely yours,

Winston Hsu Date: June 15, 2006

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